

ABSTRACT

An integrated semiconductor circuit includes a cell array havinb memory cells which can be read by word lines and bit lines. Two bit lines in each case are connected to
5 inputs of the same signal amplifier. In order to compensate for parasitic capacitances which arise at thin sidewall insulations between the patterned word lines and adjacent bit line contacts which connect the bit lines located at a higher level to the active regions located at a deeper level, two additional word lines and dummy contacts of the bit lines are dummy contacts lead past this additional word lines. The additional parasitic
10 capacitances produced by the dummy contacts alter the electrical potential of the respective reference bit line at the signal amplifier in the same way as the parasitic capacitances of activated bit lines, as a result of which the measured differential potential is corrected with respect to the parasitic effects.